Direct Sub-μm Lateral Patterning of SOI by Focused Laser Beam Induced Oxidation *

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We have developed a method for resistless patterning of Silicon-On-Insulator (SOI) in order to directly achieve lateral dielectric isolation. Our method employs a diffraction limited laser spot of a cw argon laser which is scanned across the SOI surface and directly oxidizes the silicon in ambient atmosphere. We investigate the dependence of the line width on the laser power and laser wavelength and scanning speed by AFM measurements. Line widths as narrow as 200 nm are achieved. We have fabricated in-plane-gate transistors with effective channel widths of 250 nm and excellent gate to source-drain isolation. We further demonstrate how our method can be extended for local simultaneous oxidation and doping of the silicon surface with high spatial resolution. A novel in-plane-FET device has thus been realized.

1. INTRODUCTION

Silicon-on-insulator (SOI) CMOS has several advantages as compared to conventional CMOS, amongst which are the dielectric isolation of the devices, thus preventing latch-up, and a substantial reduction of parasitic capacitance, communication delays and power consumption due to the presence of only vertical junctions. Further advantages are radiation hardness and an improved transconductance and subthreshold slope.

Besides the standard methods for lateral patterning of SOI by means of optical lithography, other methods have been developed for special purposes. Electron beam lithography and subsequent etching is often employed for nanoscale patterning [1]. Crell et.al. have fabricated in-plane-gate transistors on SOI by focused ion beam implantation of Ga+ ions [2]. AFM surface oxidation of SOI was employed by Campbell et.al. to produce a mask for a subsequent etching step [3].

In our work we were driven by the idea to make use of the non linear dependence of the silicon oxidation process on the temperature. Previous work by Micheli and Boyd has shown that oxidation of bulk silicon by a cw argon laser is easily achieved [4]. Whereas in their work no special emphasis on lateral spatial resolution was made, here we aim for the smallest possible line width of the silicon oxide.

*supported by BMBF (Grant No. M2953-B2)

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2. METHOD AND MATERIAL

We use a cw argon laser at a wavelength $\lambda = 458$ nm (514 nm) which we focus through a high numerical aperture lens system to achieve a diffraction limited laser spot of 315 nm (350 nm) FWHM. A laser power controller stabilizes the laser intensity to a precision of 0.05%. Values given in the paper relate to laser powers on the sample surface. An autofocus system is to ensure a constant spot size during the writing process. The sample is moved computer controlled by a X/Y piezo table under the laser spot, scanning speeds up to 1.7 μm/sec can be achieved. Sample treatment occurs at room temperature and ambient atmosphere.

We have used several different SOI substrates for laser oxidation.

- SIMOX with 370 nm buried oxide (BOX) and nominally undoped 15 nm silicon layer
- BESOI with 195 nm buried oxide and nominally undoped 20 nm silicon layer
- Both SIMOX and BESOI where the silicon layer was doped up to $2\times10^{18}\mathrm{cm}^{-3}$.
- Both SIMOX and BESOI which were epitaxially overgrown with up to 100 nm Si or Si/Ge including different bulk or delta doping densities.

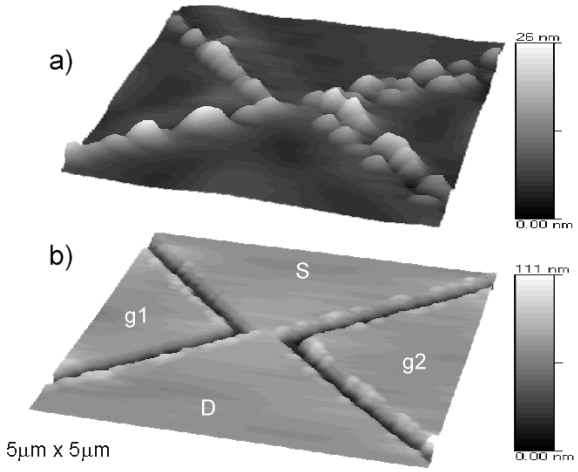

Figure 1. AFM pictures of an in-plane-gate transistor with source S, drain D and gates g1, g2 (a) before and (b) after etching the laser written oxide in diluted HF. The geometrical channel width is 600 nm, the effective channel width is smaller due to the finite line width.

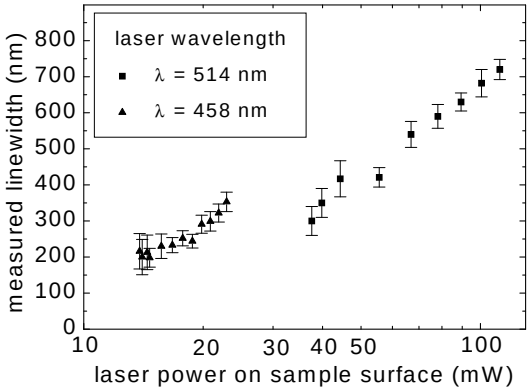

Figure 2. Measured line widths for different laser powers and for laser wavelengths of 458 nm and 514 nm obtained on a 17 nm silicon layer.

3. EXPERIMENTAL RESULTS

In this section first we discuss the surface morphology obtained by focused laser beam oxidation of the SOI surface. Second we characterize the electrical properties of oxidized lines and present two different in-plane-gate transistors.

3.1. Laser oxidation of SOI surface

An AFM picture of two adjacent V shaped lines written using $\lambda = 514\,\text{nm}$ and a laser power of 40 mW into a 20 nm SOI surface is shown in Figure 1a. The silicon surface along the trace of the laser beam appears elevated by about 20 nm in a hill shaped, irregular fashion with a width of about 1 μm. Additionally a region of about 1 μm to both sides of the trace is elevated homogeneously by a few nm. This surface morphology is common to both wavelengths. Fast scans (1.7 μm/sec) can result in a regular chain of repeated elevations and valleys along the trace with a period of 250 nm.

The hill shaped elevations appear to be thermally oxidized silicon, although there might be a contribution by non thermal, photonic oxidation [4]. The shallow elevations to both sides of the laser trace may be due to the strain induced by the oxidized line within the non oxidized silicon and/or due to debris.

After a 1 min wet etch in diluted HF all oxide is removed, see Figure 1b. The silicon surface next to the laser written line is flat and the line itself becomes apparent as a narrow, rather well defined channel. We find that oxidation is an all-or-nothing process, i.e. when oxidation takes place then the entire silicon layer is affected. Of utmost interest for sub-μm scale patterning are the line widths that can be obtained, see Figure 2. We find that the best lines that are reliably oxidized are as narrow as 200 nm, which is well below the laser spot diameter. Optimal results are obtained using $\lambda = 458\,\text{nm}$ and a laser power just above the threshold power. The threshold power sensitively depends on the silicon layer thickness, but not on the BOX thickness. As an example for $\lambda = 458\,\text{nm}$ and a silicon layer thickness of 37 nm we determined a threshold power of 25 mW, whereas for a silicon layer thickness of 100 nm only 10 mW were necessary. The threshold powers for $\lambda = 458\,\text{nm}$ are generally smaller than for $\lambda = 514\,\text{nm}$ which is due to a larger absorption coefficient in conjunction with a smaller laser spot diameter.

From the error bars in Figure 2 it can be seen that the fluctuation of the line width is generally larger close to the threshold power, where the oxidation pro-

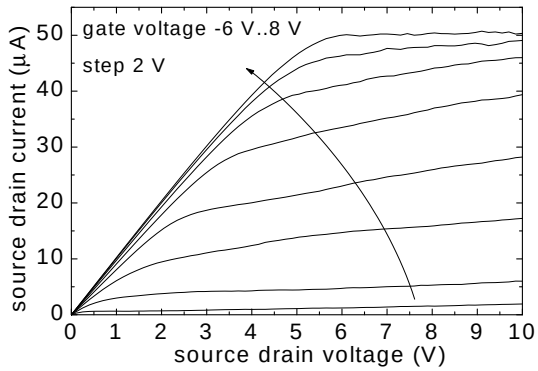

Figure 3. IPG current-voltage relation for different in-plane-gate voltages.

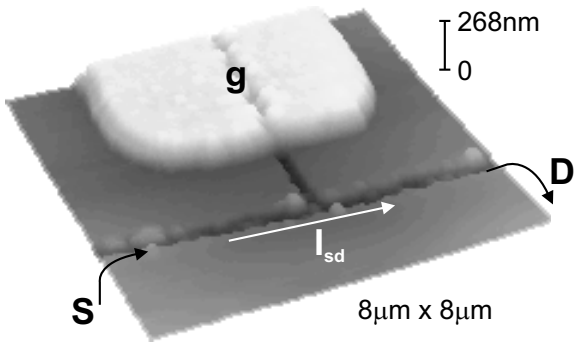

Figure 4. AFM picture of the central part of an IPFET. The gate contact (g) metalization and two orthogonal oxidized lines are visible. Alongside the longer line the source drain current I_{sd} is passed, whereas the other side is tied to the gate potential.

cess is less stable. Smoother lines are achieved for larger laser powers. Line width fluctuations of $\pm 10\%$ can then be achieved.

Further it is interesting to note that no dependence of the line width on the scan speed is found within the confidence level. We explain this observation by the stabilization of the line width by an effective self limiting mechanism. This mechanism is caused by an abrupt drop of absorption when silicon is oxidized.

3.2. In-plane-gate transistor fabricated by focused laser beam oxidation

We have fabricated in-plane-gate (IPG) transistors [2][7] in the geometry of Figure 1 in order to test the dielectric properties of the oxidized lines and to gain information about the silicon-silicon oxide interface. Leakage currents at 100 V across a 15 μm long line are in the pA range, and electrical breakthrough at higher voltages in general occurred across the BOX first. After etching the oxide to reduce the effect of charge trapping in the side walls [6] and possibly of dangling bonds we have obtained transistor action on all substrates except for highly doped samples. A Hydrogen plasma anneal for 60 min at 150 ^{o}C also improved the transconductance. In Figure 3 we show the current-voltage curve of an IPG with a geometrical channel width of 600 nm fabricated on undoped SOI. The rather high saturation voltage is due to the bad quality of the BOX on its upper interface where an electron inversion channel was induced by the back gate. The electron density was 4×10^{12}cm^{-2} at a back gate voltage of 50 V. Hole channels showed a similar behavior. The narrowest IPGs we have been able to reliably fabricate had a geometrical channel width of 450 nm, which leaves an effective channel width of 250 nm assuming a line width of 200 nm. The fact that in even narrower IPGs the source drain channel was closed may be due to a) enhancement of the line width in the vicinity of another line due to a reduced thermal conductivity and b) degradation of the silicon directly adjacent to the silicon oxide. We note that the IPGs showed a slight hysteresis when sweeping the gate voltage which might be due to carrier trapping in the silicon-silicon oxide interface.

3.3. IPFET by combined laser beam oxidation and codoping

We have extended our work to achieve not only local oxidation but also local doping of the silicon surface. For that purpose we deposit by spin-on technique a silicon dioxide film containing appropriate doping atoms onto the silicon surface. Thus when heating the surface by the focused laser beam, doping atoms are diffused into the silicon layer [7]. We observe that undoped SOI becomes conductive along

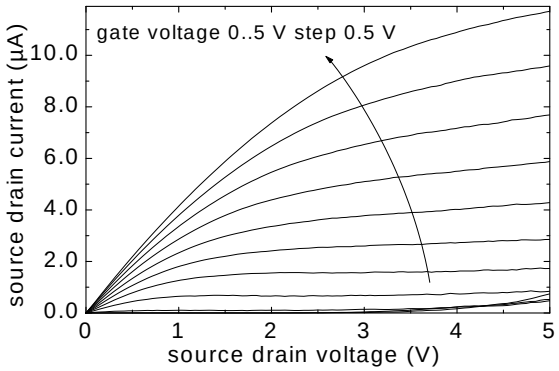

Figure 5. IPFET current-voltage relation for side-gate voltages from 0 to 5 V.

a laser oxidized line even when the line is interrupted by gaps up to 500 nm in length. This means that oxidation is accompanied by codoping in close vicinity with an extent of about 150 nm. In other words electrically isolating lines can be generated while simultaneously a very confined region of only 150 nm to both sides is doped. The doping concentration and conductivity increase with decreasing writing speed.

We have fabricated a novel 'In-Plane Field Effect Transistor' (IPFET) by making use of this technique. An AFM picture of part of the device is shown in Figure 4. The source drain current is conducted along one side of the oxidized line, whereas to the other side the gate voltage is applied. We have fabricated normally ON and normally OFF IPFETs by appropriately choosing the laser scan speed. The current voltage relation of a normally OFF IPFET is shown in Figure 5. At zero gate voltage no source drain current is observed, whereas at a gate voltage of 1.5 V the IPFET turns on. Saturation can be observed even though the source drain current is passed in close vicinity to the laser induced oxide.

4. CONCLUSION

In summary we have developed a novel method which allows the direct resistless patterning of thin film SOI. The method employs a focused cw laser beam which locally oxidizes the silicon layer. Line widths as low as 200 nm can reliably be generated by appropriately choosing wavelength, laser power and scanning speed. Electrical isolation across oxidized lines is excellent. We have demonstrated the method by the fabrication of functional IPG transistors with geometrical channel widths as narrow as 450 nm. Additionally we have extended our work to local oxidation with codopig. A novel in-plane field effect transistor has thus been fabricated. The quality of the laser induced oxide may be improved further by oxidation in pure dry oxygen.

REFERENCES

1. E. Leobandung, L. Guo, Y. Wang and S. Chou. Appl. Phys. Lett. 67, 938 (1995)
2. C. Crell, K. Wieczorek, H.-U. Schreiber, A. D. Wieck. Appl. Phys. Lett. 68, 2538 (1996)
3. P. M. Campbell, E. S. Snow, P. J. McMarr. Appl. Phys. Lett. 66, 1388 (1995)
4. F. Micheli and I. W. Boyd. Appl. Phys. Lett. 15, 1149 (1987)
5. G. J. Willems, J. J. Poortmans and H. E. Maes. J. Appl. Phys. 65, 3408 (1987)
6. P. C. Karulkar in: Silicon-On-Insulator Technology and Devices, Ed. S. Cristoloveanu, The Electrochemical Society 1994, page 209
7. P. Baumgartner et.al. Appl. Phys. Lett. 64, 592 (1994)