

## Vertical field effect transistors realized by cleaved-edge overgrowth

F. Ertl <sup>a</sup>, T. Asperger <sup>a</sup>, R. A. Deutschmann <sup>a</sup>, W. Wegscheider <sup>a,b</sup>,

M. Bichler <sup>a</sup>, G. Böhm <sup>a</sup>, and G. Abstreiter <sup>a</sup>

<sup>a</sup> Walter Schottky Institut, Technische Universität München, Am Coulombwall 3,

D-85748 Garching, Germany

<sup>b</sup> Institut für Angewandte und Experimentelle Physik, Universität Regensburg,

Universitätsstraße 31, D-93040 Regensburg, Germany

**Abstract:** We present a brief survey of vertical transistor devices fabricated by the cleaved-edge overgrowth technique. Different device types are realized using different transistor substrates grown by molecular beam epitaxy. These substrates mainly vary in the layer sequence and thickness between the source/drain contacts. Common to all designs is the vertical gate structure overgrown on a cleavage plane of the substrates. By biasing the gate a two-dimensional electron system of tunable density is induced between source/drain. We study the DC transport properties of long-channel (source-drain distance  $\sim 1 \mu\text{m}$ ) as well as short-channel (source-drain distance  $\sim 50 \text{ nm}$ ) devices. Also the choice of the source/drain isolation (a superlattice or a  $p^+-\delta$ -doping or a hetero barrier) affects the characteristic device behavior.

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**Corresponding author:** Frank Ertl, Walter Schottky Institut, Technische Universität München, Am Coulombwall 3, D-85748 Garching, Germany, phone: +49 89 28912778, fax: +49 89 3206620, email: [ertl@wsi.tum.de](mailto:ertl@wsi.tum.de)

## 1. Introduction

Over the last decade the cleaved-edge overgrowth technique, first successfully demonstrated by Pfeiffer *et al.* [1], remained a source of novel sample structures with highest crystalline quality. The method relies on subsequent molecular beam epitaxy growth steps in different orthogonal crystal directions, which are created by *in-situ* cleaving the sample. Especially the electrical and optical investigation of low-dimensional electron systems, like quantum wires [2,3] (Luttinger liquid behavior) or quantum dots [4] (coupled artificial atoms) tailored with atomic precision, took advantage of the technique. Also new possibilities to study two-dimensional electron transport opened up, see for example [5] (tunneling into fractional quantum Hall edges) and [6] (periodically modulated two-dimensional electrons).

In this paper we focus on vertical transistor devices realized by cleaved-edge overgrowth, that are subject to DC transport studies dependent on several design parameters (e.g. channel length and thickness). We compare several concepts to insulate source/drain and thus guide electrons in the channel with each other, which includes superlattice,  $p^+$ - $\delta$ -doped and hetero source/drain barriers.

## 2. Experimental

We employ molecular beam epitaxy in the lattice-matched AlGaAs/GaAs material system to grow the different transistor substrates on semi-insulating (001)-GaAs wafers. All samples have a insulating potential barrier sandwiched between two  $1\ \mu\text{m}$  thick  $n^+$ -GaAs source/drain contacts in common; only the particular type of barrier as shown in Fig. 1 varies. We involve an AlGaAs/GaAs superlattice, a simple AlGaAs hetero barrier, a  $p^+$ - $\delta$ -doped GaAs barrier and a GaAs embedded AlGaAs hetero barrier in our investigation. For details on the grown structure refer to the corresponding part in the results section. The geometric channel length  $L$  of the transistor is defined by the thickness of the grown barrier, which can be controlled nearly within one monolayer. The device is denoted as long-channel if the source-drain distance is  $L \sim 1\ \mu\text{m}$  and as short-channel for  $L \sim 50\ \text{nm}$  in our case. Pieces of the transistor

substrates are returned into growth chamber and cleaved under ultra-high vacuum conditions. Immediately afterwards we overgrow the freshly exposed (110) cleavage plane with a layer sequence common to all samples. At first the i-GaAs electron channel with a thickness  $QW$  is deposited, followed by an AlAs gate barrier and the  $n^+$ -GaAs gate contact. After the growth a mesa is etched on the (100) surface and ohmic Pd/Ge/Au contacts are attached to all terminals.

We characterize all samples by measuring the current-voltage relation while the gate is biased. In our setup either the top (short channel device) or bottom (long channel device) contact is grounded and the source-drain voltage is applied to the remaining one. The source-drain current is measured while simultaneously the voltage drop across the channel is recorded in 4-point-probe configuration.

### 3. Results

The output characteristics of two long-channel devices are presented in Fig. 2, which both have a channel length of  $L=3\ \mu\text{m}$  and thickness  $QW=20\ \text{nm}$ . Fig. 2(a) shows the results for a device with a superlattice used as barrier (Fig. 1(a)), which has a 15 nm period consisting of 12 nm GaAs and 3 nm  $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ . Fig. 2(b) displays data of a transistor with bulk  $\text{Al}_{0.06}\text{Ga}_{0.94}\text{As}$  barrier (Fig. 1(b)), which matches the mean Al-content of the superlattice. In experiment we set the sample temperature to 800 mK to explore quantum effects in the DC transport.

The I-V curves of the superlattice device exhibit a strong slope for source-drain voltages up to 75 mV in the linear regime and a nearly perfect saturation for voltages greater than 150 mV. Around 100 mV source-drain voltage the I-V traces feature a negative differential resistance region. The superlattice acts as a barrier between source-drain, but also modifies transport in the electron channel by the remote potential. Thus the two-dimensional electron system in the channel undergoes a weak periodic density modulation, which causes back folding of the electrons band structure. In an electrical field these electrons are accelerated

towards the Brioullin zone boundary in k-space and eventually become Bragg reflected, which leads to electron localization and negative differential resistance. We refer to Ref. [7] for an extensive discussion focusing on the superlattice influence. In comparison the device including the simple hetero barrier shows a weaker slope in the linear region and a small rise with source–drain voltage in saturation regime. We find no signs of a negative differential resistance, since no periodic density modulation is apparent. To shortly sum it up, the output behavior of the long-channel devices can be improved with respect to the saturation and linear regime by choosing a superlattice barrier.

Measurements of vertical short-channel transistors with a  $6 \cdot 10^{12} \text{ cm}^{-2}$  planar  $p^+$ - $\delta$ -doped barrier in a 100 nm GaAs matrix (Fig. 1(c)) are depicted in Fig. 3. Electrostatic depletion in the contact regions flanking the  $p^+$ - $\delta$ -spike leads to an effective channel length  $L_{eff}=70 \text{ nm}$ , which can be obtained by examining the source-drain capacitance. We present data from  $QW=40 \text{ nm}$  thick devices at different temperatures of 4.2 K in Fig. 3(a) and 300 K in Fig. 3(b).

The output characteristic shows typical sub threshold behavior indicated by the diodic curves at both temperatures, much like in similar Si-based devices [8]. For gate voltages below 0.7 V the vertical transistors stay in the turned-off regime; above that value gate leakage becomes intolerably high. At low temperature we find that the device behavior is dominated by punch-through of electrons. At positive drain voltage the effective barrier height in the channel, also created by electrostatic depletion of the  $p^+$ - $\delta$ -doping, is reduced and electrons can travel from source to drain by tunneling. At higher temperatures an additional thermally activated tunneling current appears across the channel barrier. Both contributions can be recognized in Fig. 3, as the diodic curves shift either with gate voltage at constant temperature or vice versa. Although this design type is fully room temperature operable, it lacks the turned-on regime yet. In order to solve this the depletion of the  $p^+$ - $\delta$ -spike within the channel has to be compensated by simply  $n^+$ - $\delta$ -doping the channel or the gate barrier near the channel.

In Fig. 4 we show experimental data at 4.2 K of another short-channel device including an 50 nm  $\text{Al}_{0.45}\text{Ga}_{0.55}\text{As}$  hetero barrier embedded in 50 nm GaAs (Fig. 1(d) ) on each side. In this case the geometrical channel length is  $L=50$  nm and the thickness is  $QW=20$  nm in Fig. 4(a) respectively  $QW=40$  nm in Fig. 4(b).

Above a small positive gate voltage of approx. 50 mV this device type operates in the turned-on transistor state and the current-voltage relation possesses a quasi-saturated region. The loss of complete saturation is a typical short-channel effect, that emerges when shrinking down the source-drain distance. This experimental finding agrees well with non-equilibrium numerical simulations performed for this special device configuration [9]. A closer look at the onset of the quasi-saturation region reveals that it shifts linearly to higher source-drain values by increasing the gate voltage. This behavior is different from that of the long-channel device in Fig. 2, where the onset nearly stays at a constant value, or to the conventional MOSFET device, where the onset follows a square law. When the channel thickness is raised, even though the channel cross section is increased, we observe an unexpected decrease in the average source-drain current. We explain this observation by additional serial resistances stemming from the contact-channel coupling as the electron gas is located further away from the contacts at larger channel thicknesses. In order to minimize the present short-channel effects the distance between the  $n^+$ -contact regions and the gated short-channel have to be increased. By that means a design type with a short gate attached to a long-channel [10] is more favorable than a short-channel covered the whole distance by a gate.

#### **4. Conclusion**

In summary we have shown that a variety of vertical transistor devices can be fabricated using the cleaved-edge overgrowth method. Common to all transistors is the gate structure allowing us to induce a two-dimensional electron system of tunable density connecting source/drain. Devices with long electron channels ( $L\sim 1\ \mu\text{m}$ ) possess overall normal transistor operation. Additionally the superlattice device type exhibits a negative differential resistance in the

output characteristics. In comparison the superlattice type has an improved performance in comparison to the simple hetero barrier type. Short-channel ( $L \sim 50$  nm) vertical transistors were realized with planar  $p^+$ - $\delta$ -doping and embedded hetero barriers. The  $p^+$ - $\delta$ -doped devices were fully room temperature operable, but nevertheless only in the turned-off regime yet. The transistors using a hetero barrier clearly exhibit short-channel effects in the low-temperature I-V-traces, a problem which can only be overcome by a major design change.

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## Figure captions:

**Fig. 1 :** Sample structure of a vertical transistor fabricated by the cleaved-edge overgrowth method. The different design types vary in the section marked by the circle. Following kinds of source/drain separation layers are under investigation: (a) a AlGaAs/GaAs superlattice, (b) a simple AlGaAs hetero barrier, (c) a  $p^+-\delta$ -doped GaAs separator and (d) an embedded AlGaAs hetero barrier.

**Fig. 2 :** Output traces of a transistor device with (a) a superlattice in comparison with (b) a simple hetero barrier. Both transistors have a channel length of  $L=3\ \mu\text{m}$  and thickness of  $QW=20\ \text{nm}$ . The superlattice consists of 12 nm GaAs and 3 nm  $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$  per 15 nm period. The simple  $\text{Al}_{0.06}\text{Ga}_{0.94}\text{As}$  hetero barrier matches the average Al-content of the superlattice.

**Fig. 3 :** Typical device characteristics of a vertical transistor with a  $6\cdot 10^{12}\ \text{cm}^{-2}$   $p^+-\delta$ -doped barrier at (a) 4.2 K or (b) 300 K. The channel possesses an effective length of  $L_{\text{eff}}=70\ \text{nm}$  and a thickness of  $QW=40\ \text{nm}$ .

**Fig.4 :** Current-voltage relation of samples equipped with an  $\text{Al}_{0.45}\text{Ga}_{0.55}\text{As}$  hetero barrier at 4.2 K. The channel is (a)  $QW=20\ \text{nm}$  or respectively (b)  $QW=40\ \text{nm}$  thick at constant geometric length of  $L=50\ \text{nm}$ .

Figure 1:

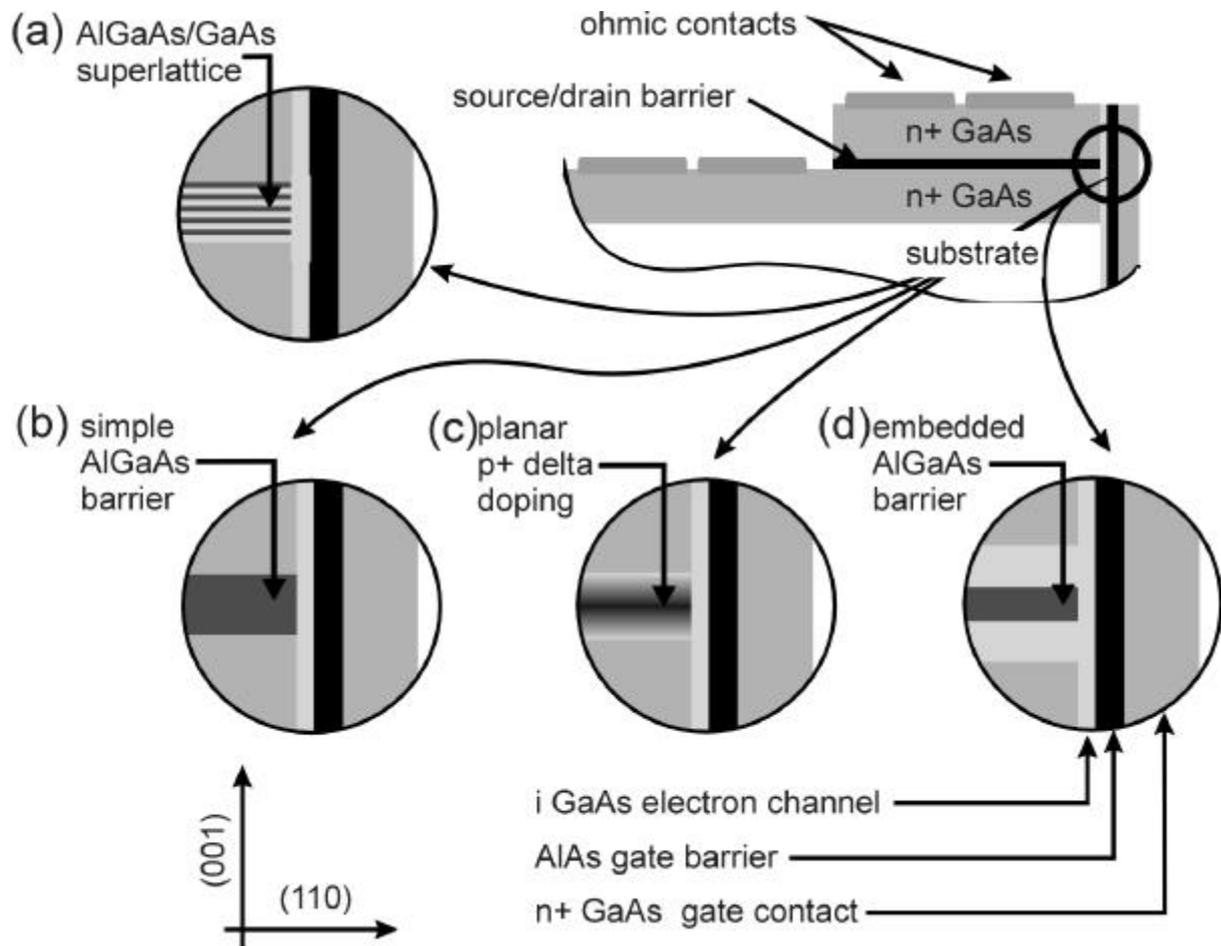


Figure 2:

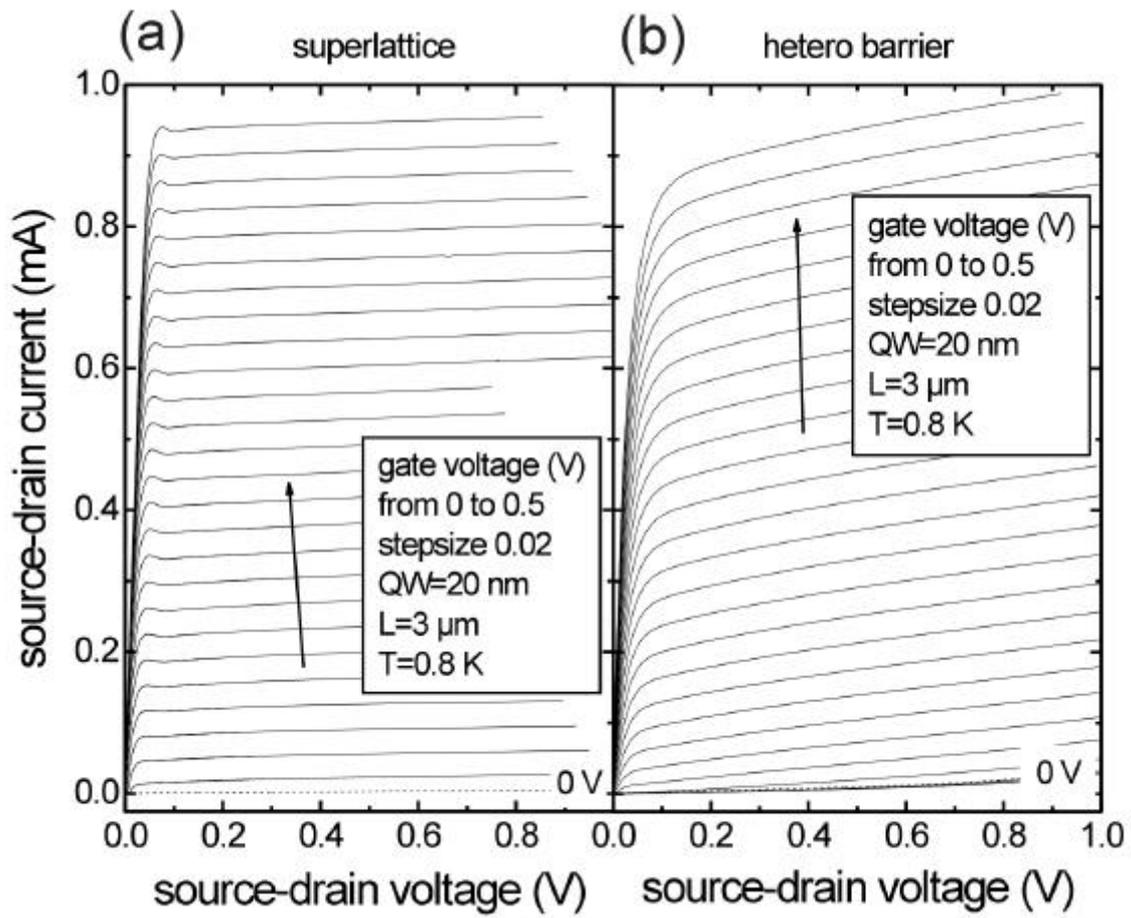


Figure 3:

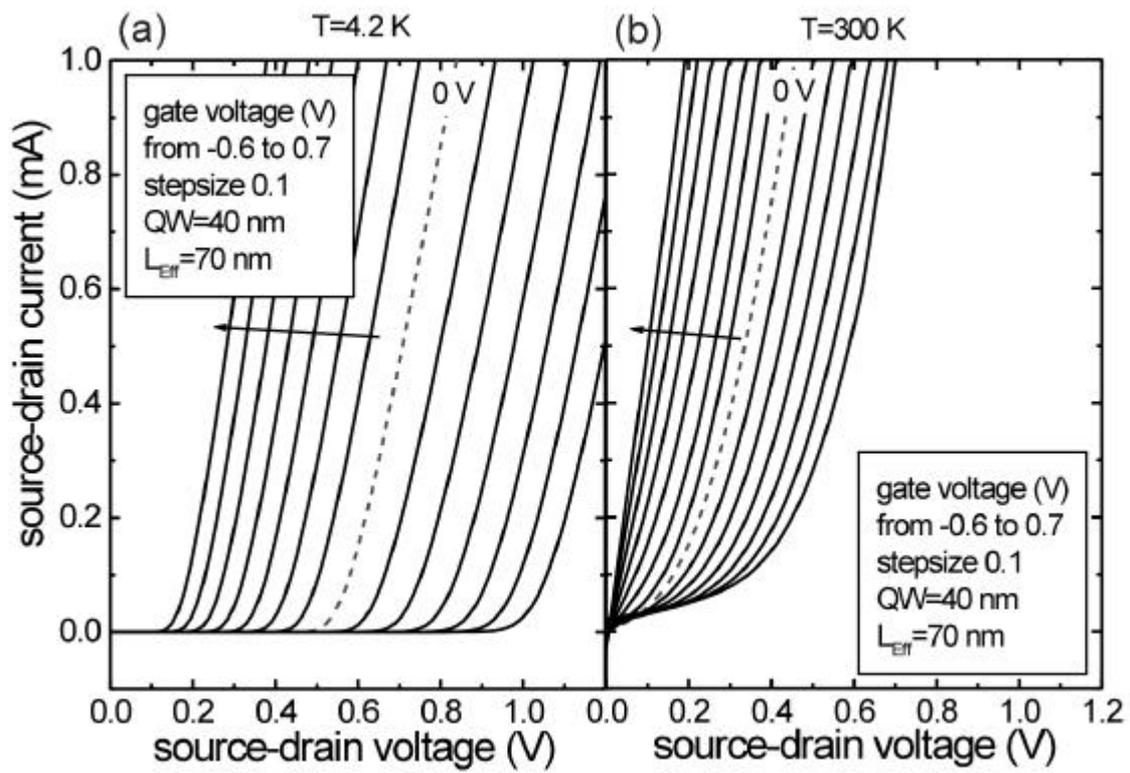


Figure 4:

